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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,494	08/03/2000	Salil R. Raje	MDS-P007	1465

7590 05/21/2003

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EXAMINER
LEVIN, NAUM B

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,494	RAJE ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment (Paper No.6)* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36,70-81 and 94-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36,70-81 and 94-100* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office action is in response to application 09/632,494 and amendment filed on 03/17/2003. Claims 1-36, 70-81 and 94-100 remain pending in the application.

2. Applicant has amended claims 14-24, 76 and 94, and canceled claims 37-69 and 82-93.

Based on the amendment Examiner performed additional search, and has found a new reference.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-36, 70-81 and 94-100 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyle et al. (US Patent 6,557,145).

Boyle discloses method for design optimization using logical and physical information including:

(1), (13), (25) A method, computer-readable medium with code and computer system of performing a design of an integrated circuit comprising:

defining a physical design/layout of the circuit while tracking an error (timing hot spots/slacks) in prediction of a timing value associated with one or more

nets/interconnects in the circuit (timing analysis) (col.2, ll.14-21; col.3, ll.51-67; col.4, ll.1-4 and ll.54-58; col.20, ll.62-67 and col.21, ll.1-16); and

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold (col.4, ll.55-62 and col.6, ll.19-41);

(2), (14), (26) The method, computer-readable medium with code and computer system, wherein the defining the physical design further comprises performing a soft placement of the design (col.6, ll.32-37);

(3), (15), (27), (71), (77), (100) The method, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.1, ll.40-67; col.42 ll.1-12);

(4), (16), (28), (72), (78), (99) The method, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.5, ll.7-31);

(5), (17), (29) The method, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

localizing placement of cells and wires in the physical design (col.6, ll.50-65);

creating a profile of the wire lengths from the physical design (col.10, ll.1-6; col.11 and ll.9-40);

calculating an error in a prediction of a timing value from the profile of the wire lengths (col.9, ll.66-67 and col.11, ll.9-40); and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38);

(6), (18), (30), (75), (79), (81) The method, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins/quanto-clusters (col.9, ll.40-67);

(b) localizing placement of cells and wires of the physical design into the bins (col.6, ll.50-65);

(c) creating a profile of the wire lengths in each of the bins (col.10, ll.1-6; col.11 and ll.9-40);

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively (col.9, ll.66-67 and col.11, ll.9-40);

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either (col.11, ll.63-67; col.12, ll.1-5 and col.14, ll.20-38):

further quadrisectioning the physical design and repeating (b through e) (col.14, ll.39-56);

or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold (col.14, ll.57-66);

(7), (19), (31) The method , wherein the creating a profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins (col.4, ll.62-67; col.10, ll.1-6; col.11 and ll.9-40);

(8), (20), (32) The method of, further comprising performing interactive optimization of the physical design after the error in prediction of the timing value satisfies the predetermined threshold (col.5, ll.17-23 and col.6, ll.25-40);

(9), (21), (33) The method of, further comprising analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity (col.1, ll.24-27; col.6, ll.46-48; col.15, ll.66-67 and col.16, ll.1-9);

(10), (22), (34), (97) The method of claim 9, further comprising generating a report indicative of the congestion, timing, power, signal integrity of the physical design (col.3, ll.57-61);

(11), (33), (35), (73), (74), (80) The method, further comprising:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit (col.2, ll.45-50 and col.5, ll.29-31); and

generating a GDS file from the second physical design of the circuit (col.2, ll.45-50 and col.5, ll.29-31);

(12), (24), (36) The method, wherein the performing the second physical design of the circuit further comprises simultaneously performing one or more of the following in to parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.3, ll.66-67 and col.4, ll.1-4);

(70), (76) A method for a first party to fabricate a semiconductor device, comprising:

receiving an sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit (col.1, ll24-27; col.2, ll.14-21; col.3, ll.51-67; col.4, ll.1-4 and ll.54-58; col.20, ll.62-67 and col.21, ll.1-16);

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold (col.4, ll.55-62 and col.6, ll.19-41); and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and after receiving the sign-off prototype, the first party performing (col.2, ll.45-50 and col.5, ll.29-31):

generating a second physical design of the circuit from the sign-off prototype (col.2, ll.45-50 and col.5, ll.29-31);

generating a GDS file from the second physical design (col.2, ll.45-50 and col.5, ll.29-31);

having a mask set generated from the GDS file (col.2, ll.45-50 and col.5, ll.29-31); and

having the semiconductor device/integrated circuit fabricated using the mask set (col.2, ll.45-50 and col.5, ll.29-31);

(94) A semiconductor device, comprising: an integrated circuit segmented into a plurality of bins, the integrated circuit including:

a first bin having a first group of nets optimized to a first set of criteria (col.1, ll24-27; col.6, ll.50-65; col.9, ll.40-67 and ll.66-67; col.10, ll.1-6; col.11, ll.9-40 and ll.63-67; col.12, ll.1-5 and col.14, ll.20-38); and

a second bin having a second group of nets optimized to a second set of criteria, wherein the first criteria and the second criteria are substantially different (col.14, ll.39-56);

(95) The semiconductor device of claim 94, wherein the first bin is designed to a first GDS level and the second bin is designed to a second GDS level (col.1, ll24-27; col.6, ll.50-65; col.9, ll.40-67 and ll.66-67; col.10, ll.1-6; col.11, ll.9-40 and ll.63-67; col.12, ll.1-5 and col.14, ll.20-38 and ll.39-56);

(96) A computer-readable medium including computer code configured to perform the design of an integrated circuit, the computer code including:

timing and placement tools that are configured to generate a prototype , the timing and placement tools including:

a resource and allocation and sharing module (col.8, ll.10-35);

an implementation module (col.9, ll.3-14);

a logic structuring module (col.8, ll.28-30);

a technology mapping module (col.10, ll.47-67; col.11, ll.1-22 and col.18, ll.55-62);

a global optimization module (col.19, ll.32-34); and

a prototype optimization tool (col.2, ll.45-50; col.5, ll.29-31 and ll.17-23 and col.6, ll.25-40); and

a prototype optimization tool that enables the optimization of the prototype (col.2, ll.45-50; col.5, ll.29-31 and ll.17-23 and col.6, ll.25-40);

(98) The computer readable medium of claim 96, wherein the resource and allocation and sharing module; the implementation module; the logic structuring module; the technology mapping module; the global optimization module; and the prototype optimization tool operate sequentially/top-down/point tools (col.2, ll.51-67 and col.3, ll.1-6).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Following references also disclose integrated circuit physical design utilizing physical placement level of the circuit using parallel process: Rostoker et al. US Patent 5,867,399; Keren et al. US Patent 5,544,071 and Rostoker et al. US Patent 5,495,419. For example Rostoker discloses a parallel placement algorithm that is executed by parallel processors, thereby shortening the time to achieve the placement function.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N L
May 14, 2003

[illegible]
PATENT EXAMINER